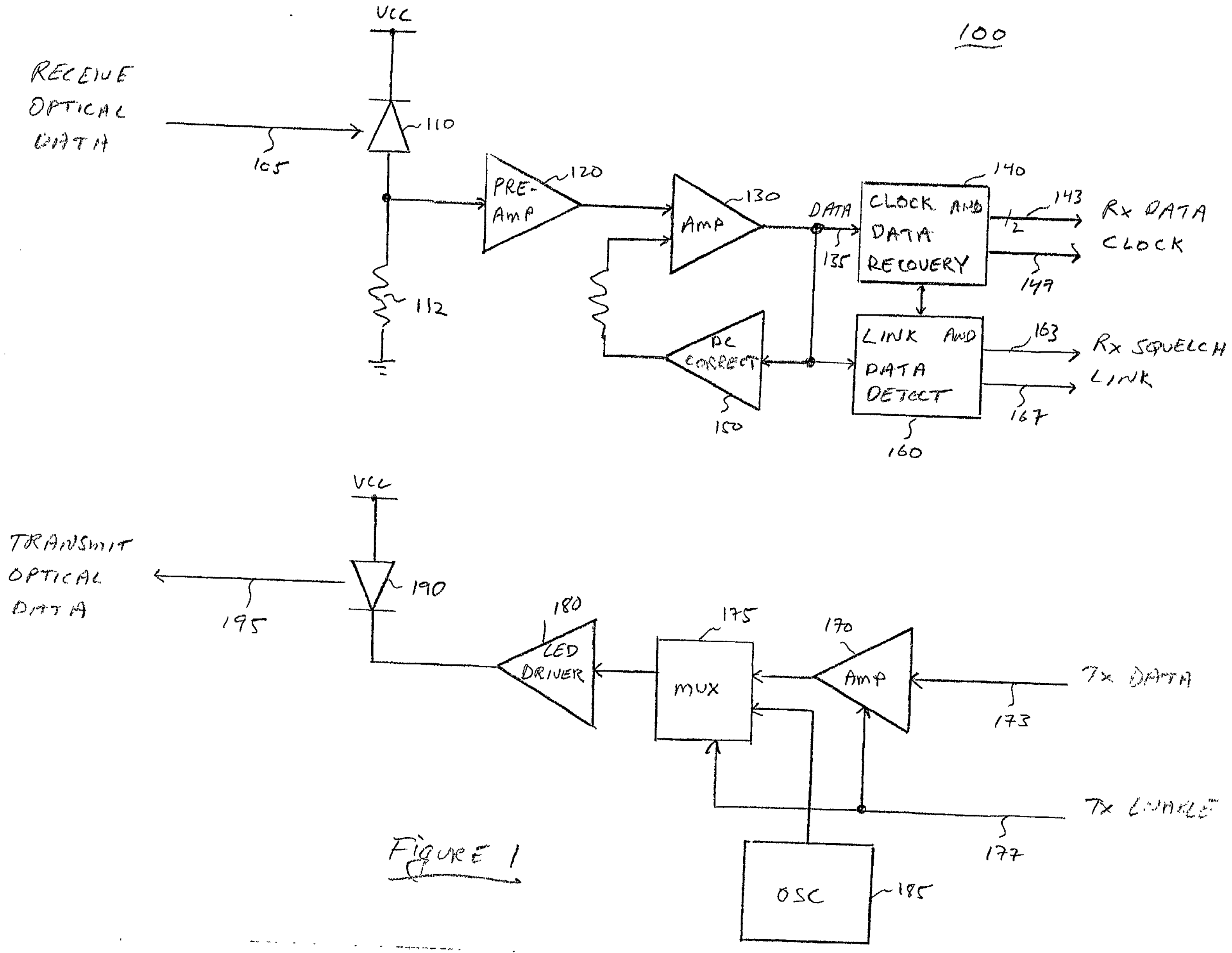
100
RECEIVE OPTICAL DATA
105
VCC
110
112
PRE-AMP
120
AMP
130
DATA
135
DC CORRECT
150
CLOCK AND DATA RECOVERY
140
2
143
Rx DATA
147
CLOCK
LINK AND DATA DETECT
160
163
Rx SQUELCH
167
LINK
TRANSMIT OPTICAL DATA
195
VCC
190
LED DRIVER
180
MUX
175
AMP
170
Tx DATA
173
Tx ENABLE
177
OSC
185

Figure 1

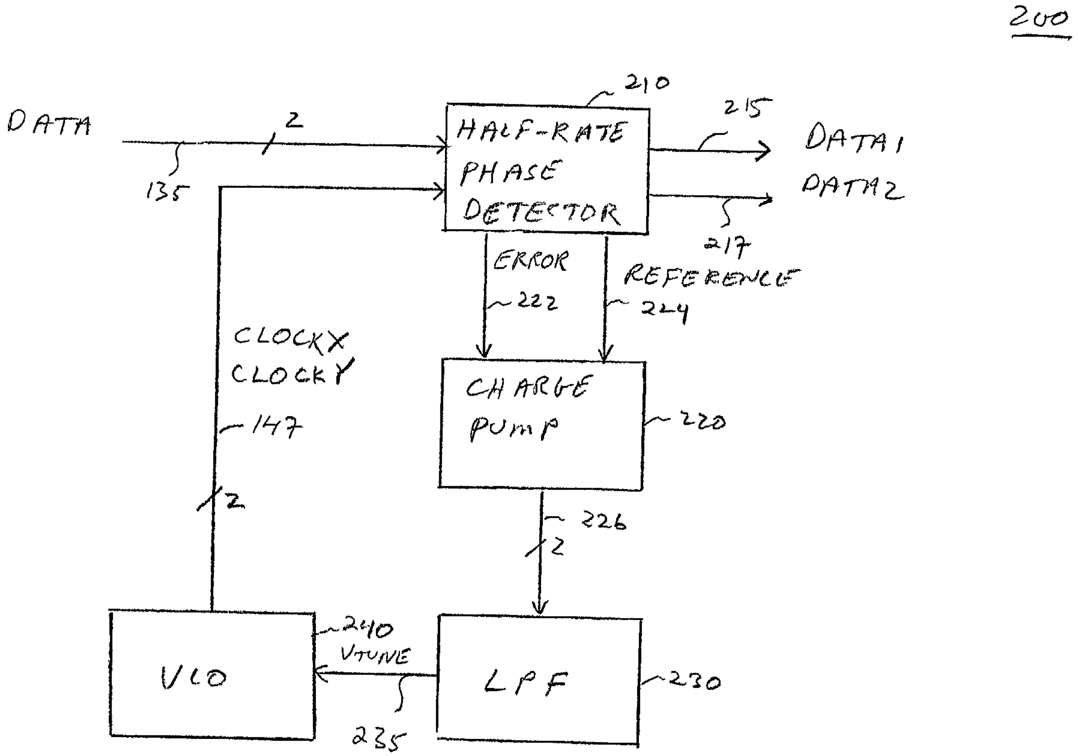
200
DATA
2
135
210
HALF-RATE PHASE DETECTOR
215
DATA1
DATA2
217
ERROR
222
REFERENCE
224
CLOCKX
CLOCKY
147
2
CHARGE PUMP
220
226
2
LPF
230
VCO
240
VTUNE
235

FIGURE 2

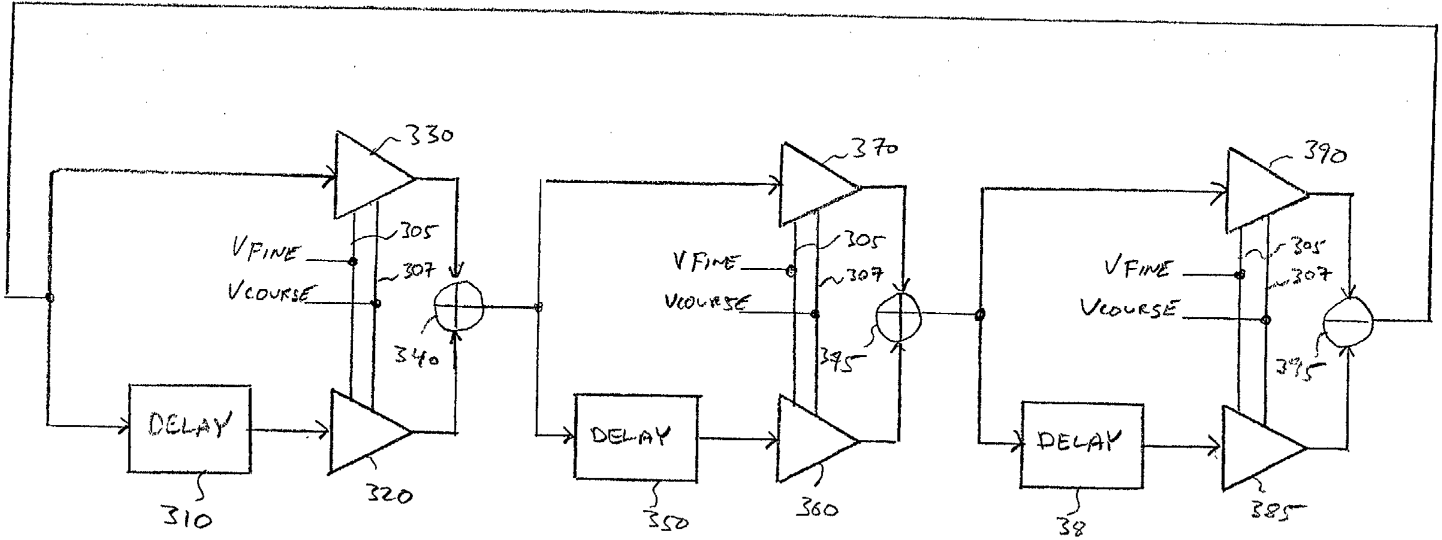
330
305
307
VFINE
VCOURSE
340
DELAY
310
320
370
305
307
VFINE
VCOURSE
395
DELAY
350
360
390
305
307
VFINE
VCOURSE
395
DELAY
38
385

Figure 3

300

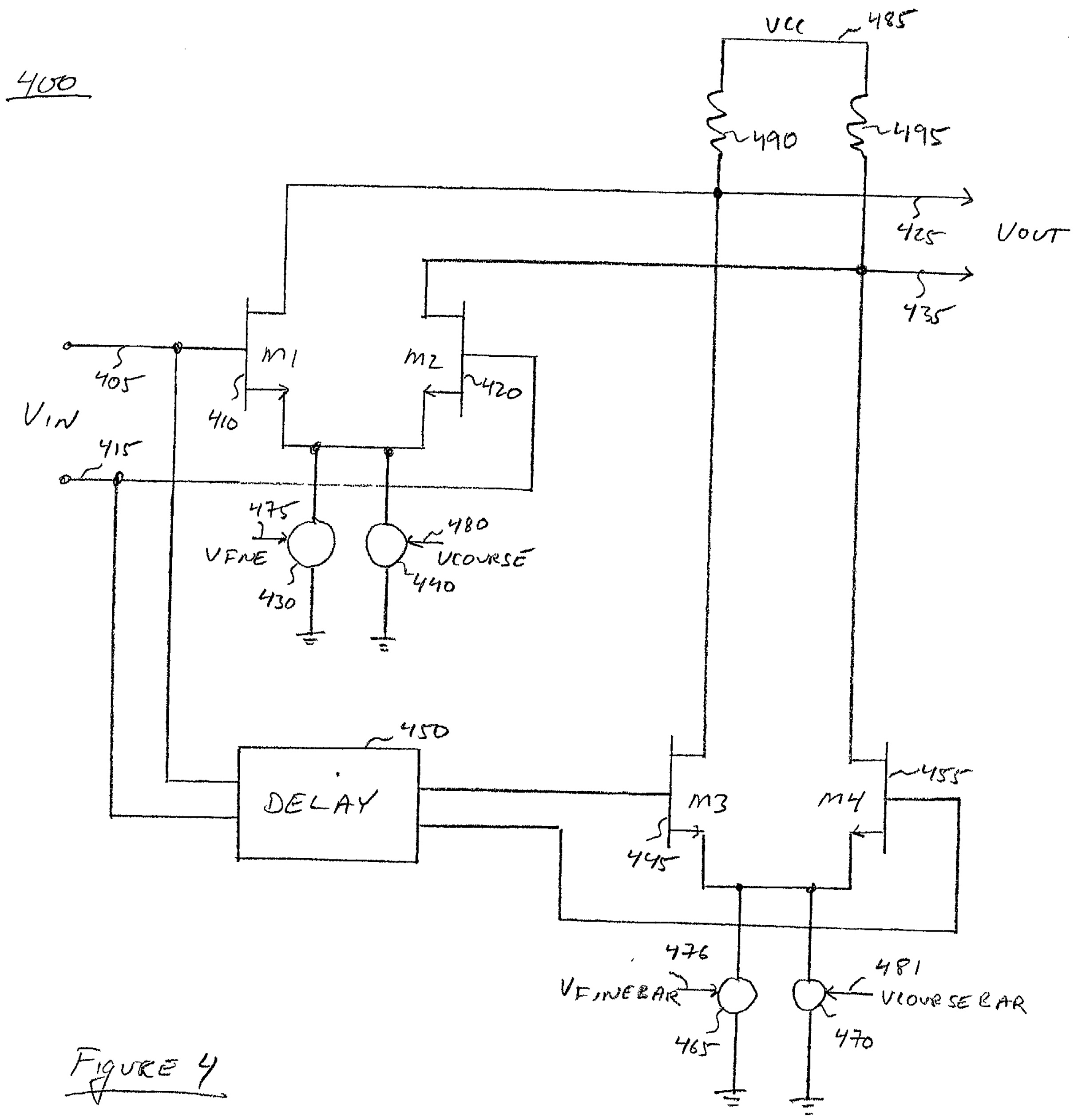
400
VCC
485
490
495
425
VOUT
435
405
VIN
415
M1
410
M2
420
475
VFINE
430
480
VCOURSE
440
450
DELAY
M3
445
M4
455
476
VFINEBAR
465
481
VCOURSEBAR
470

FIGURE 4

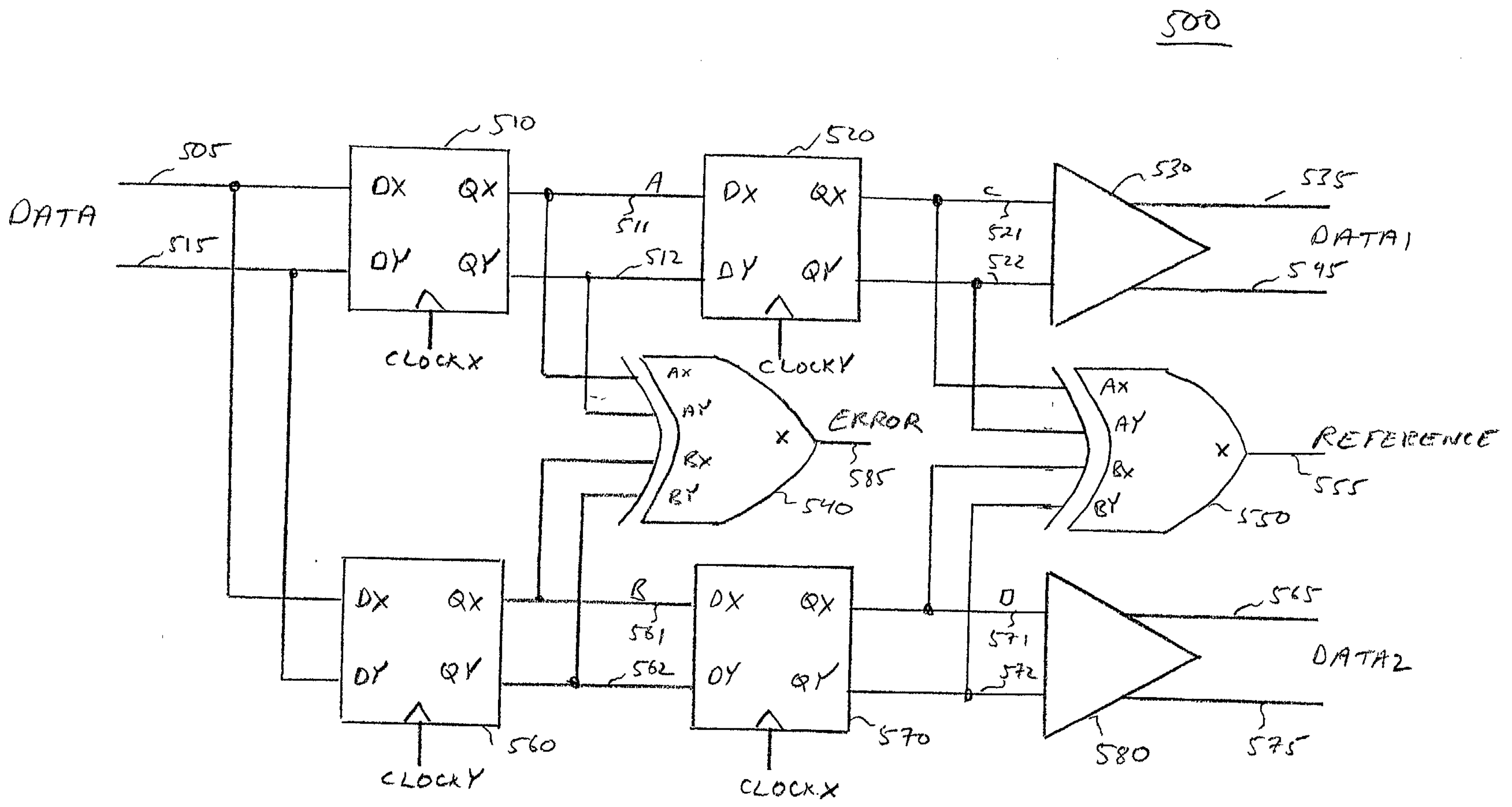
500
505
DATA
515
510
DX
QX
DY
QY
CLOCK X
A
511
512
520
DX
QX
DY
QY
CLOCK Y
C
521
522
530
535
DATA 1
545
AX
AY
BX
BY
X
ERROR
585
540
AX
AY
BX
BY
X
REFERENCE
555
550
DX
QX
DY
QY
CLOCK Y
560
B
561
562
DX
QX
DY
QY
CLOCK X
570
D
571
572
580
565
DATA 2
575

Figure 5

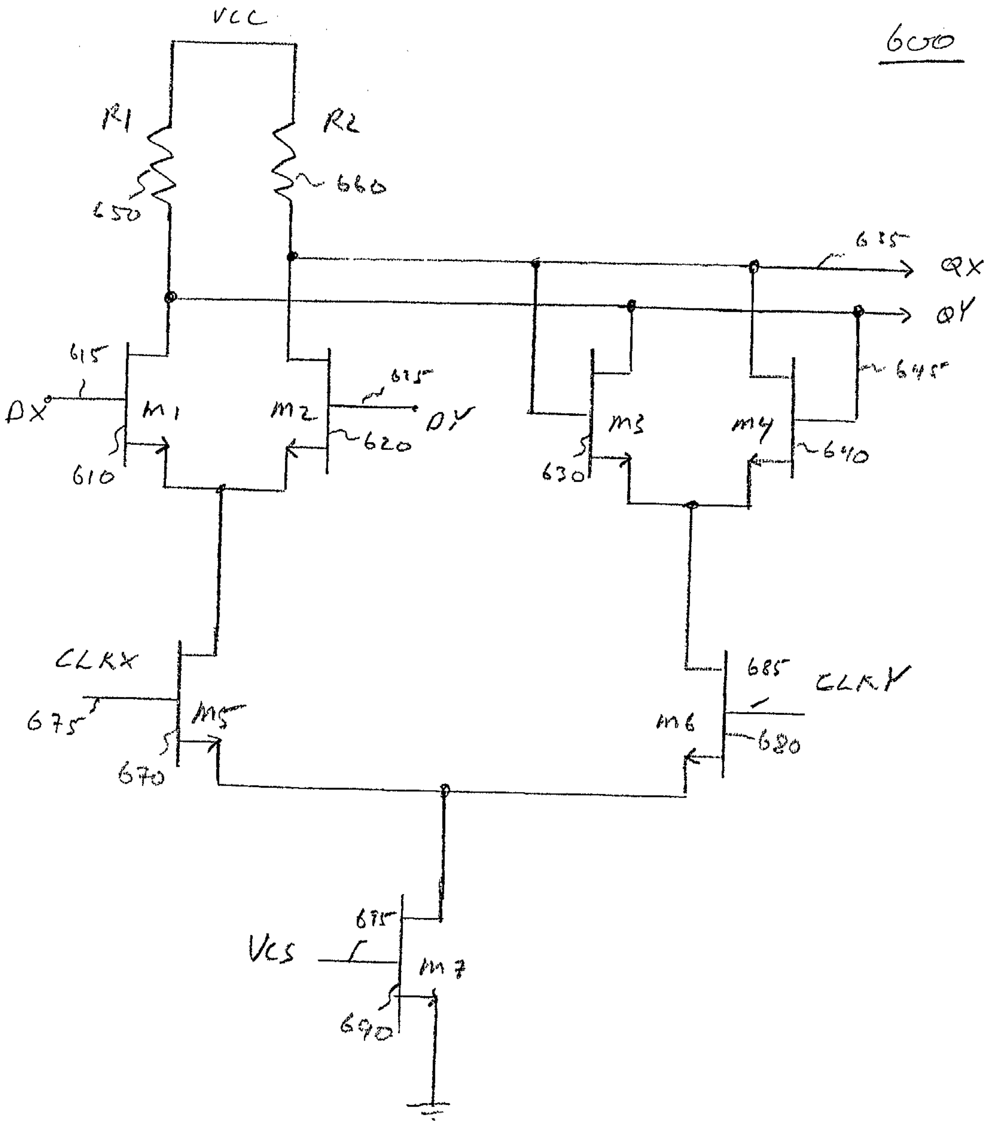
600
VCC
R1
650
R2
660
615
DX
M1
610
M2
615
DY
620
635
QX
QY
645
M3
630
M4
640
CLKX
675
M5
670
M6
685
CLKY
680
695
VCS
M7
690

Figure 6

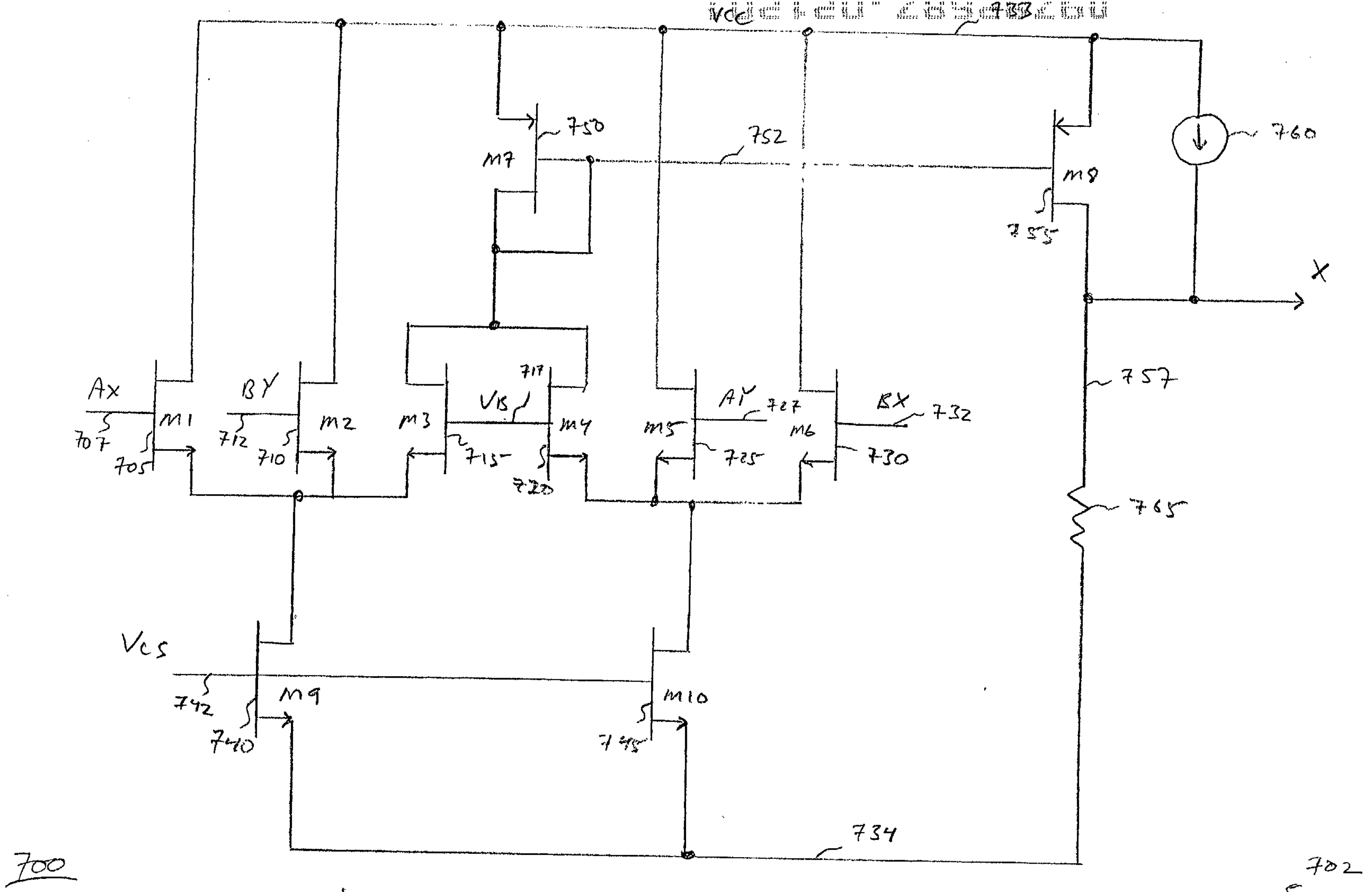

FIGURE 7B

702

A	B	$A \oplus B$	$\bar{A}$	$\overline{\bar{A}+B}$	$\bar{B}$	$\overline{A+\bar{B}}$	$\overline{(\bar{A}+B)}+\overline{(A+\bar{B})}$
0	0	0	1	0	1	0	0
0	1	1	1	0	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	0	0	0	0

FIGURE 7A

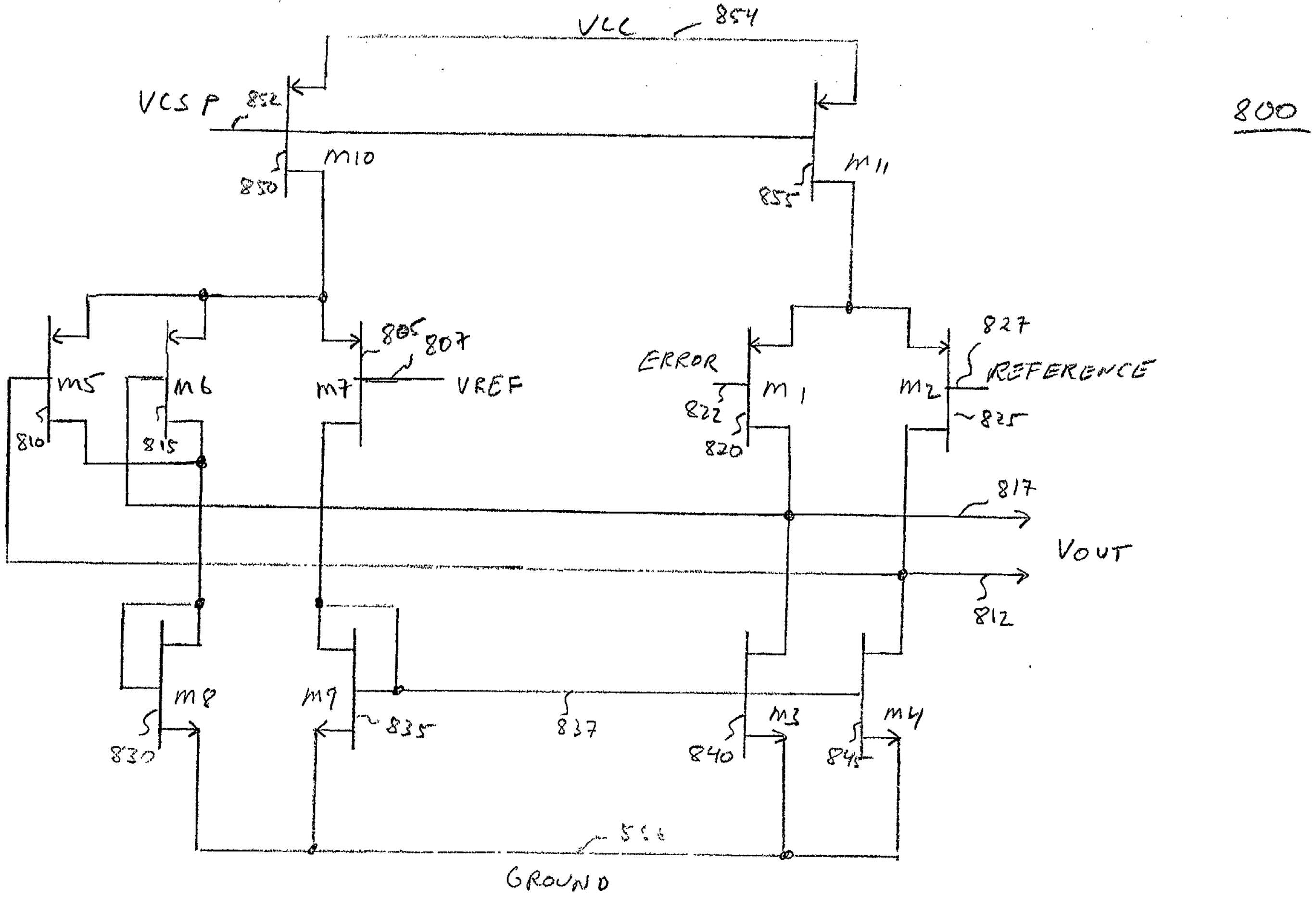
800
VCC
854
VCSP
852
M10
850
M11
855
M5
810
M6
815
M7
805
807
VREF
ERROR
822
820
M1
M2
827
REFERENCE
825
817
VOUT
812
M8
830
M9
835
837
M3
840
M4
845
556
GROUND

Figure 8

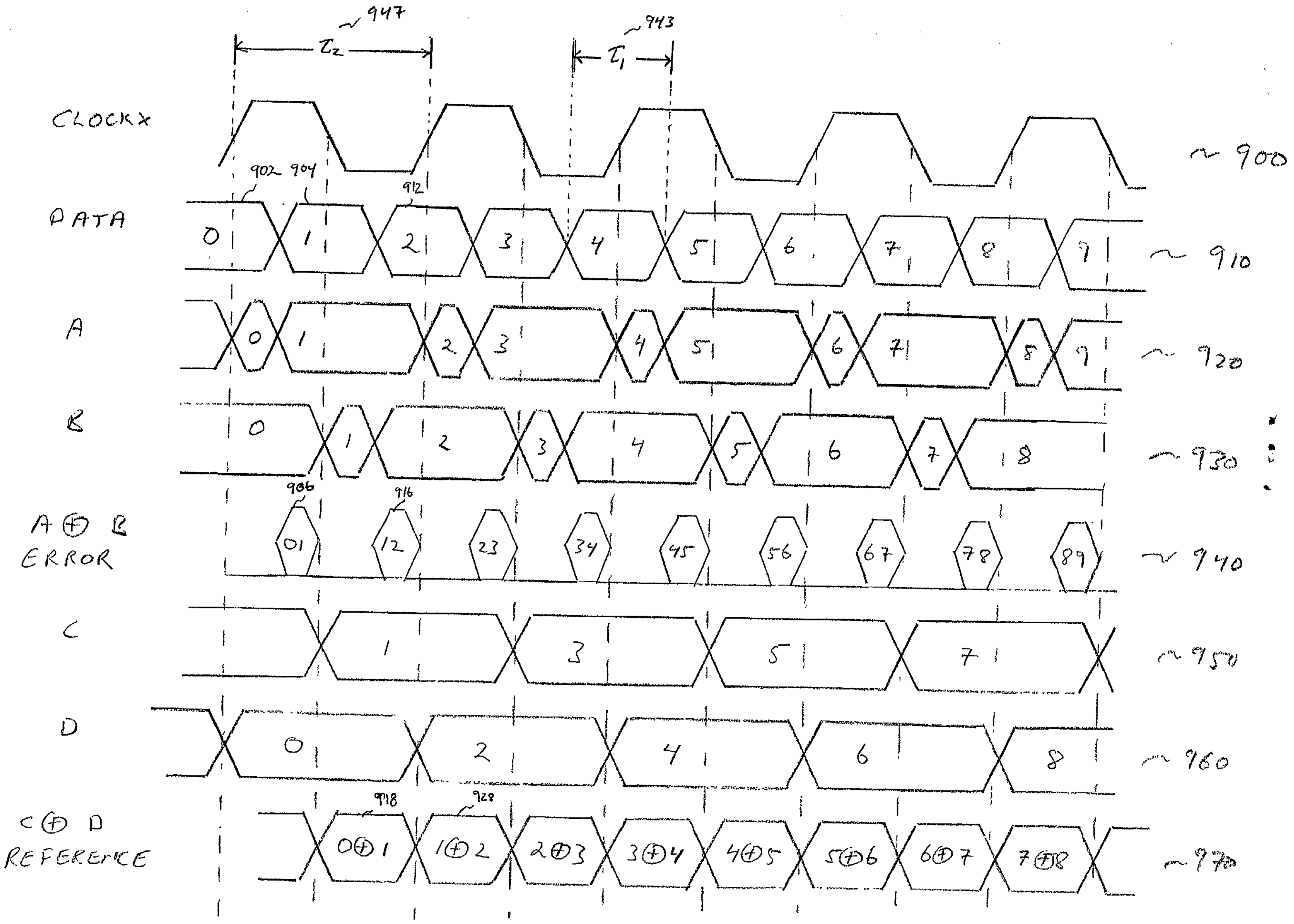
947
τ_2
943
τ_1
CLOCKX
~900
902
904
912
DATA
0
1
2
3
4
5
6
7
8
9
~910
A
0
1
2
3
4
5
6
7
8
9
~920
B
0
1
2
3
4
5
6
7
8
~930
906
916
A ⊕ B ERROR
01
12
23
34
45
56
67
78
89
~940
C
1
3
5
7
~950
D
0
2
4
6
8
~960
918
928
C ⊕ D REFERENCE
0⊕1
1⊕2
2⊕3
3⊕4
4⊕5
5⊕6
6⊕7
7⊕8
~970

Figure 9

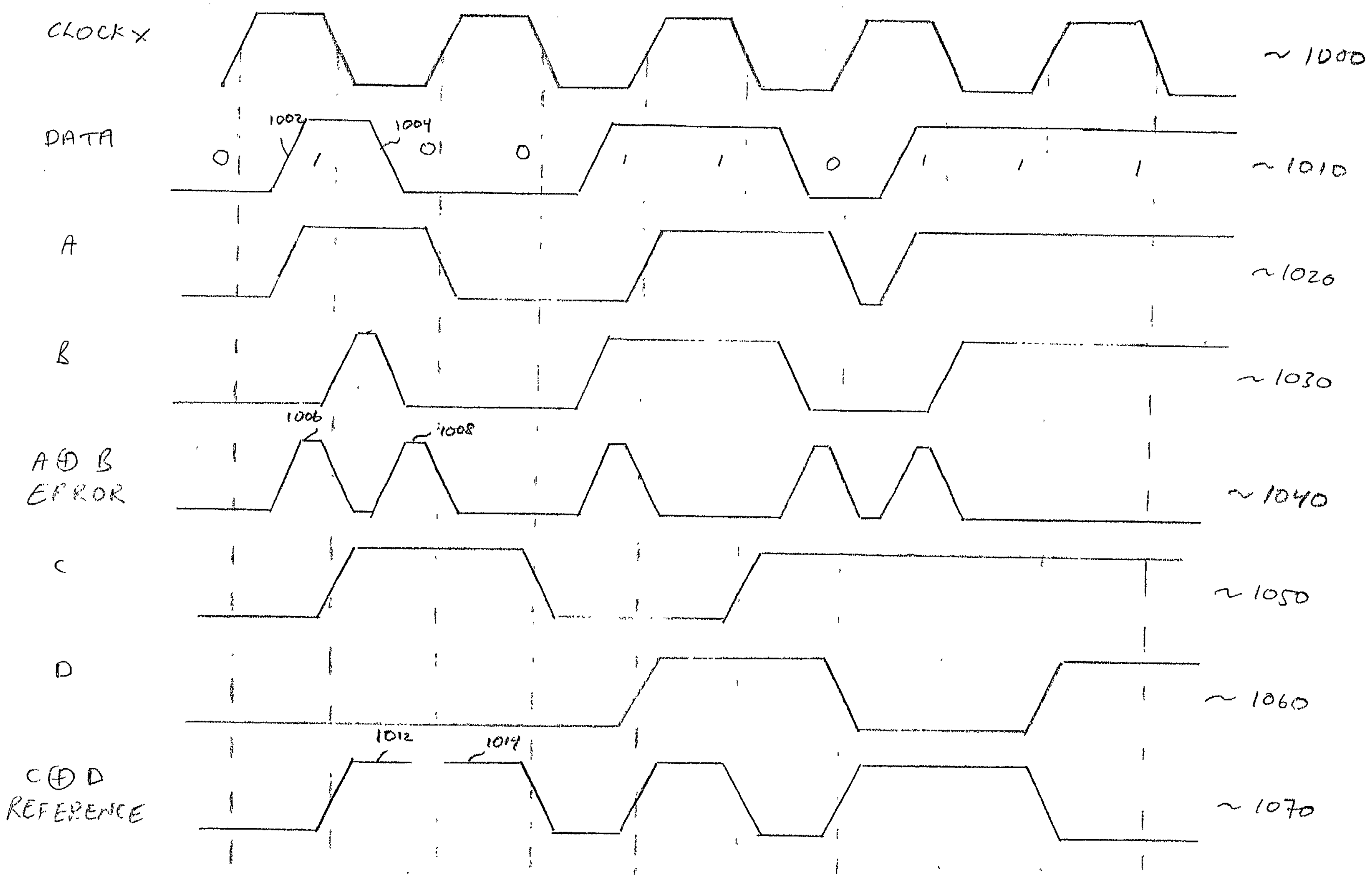
CLOCK X
~1000
DATA
0
1002
1
1004
0
0
1
1
0
1
1
1
~1010
A
~1020
B
~1030
A ⊕ B
ERROR
1006
1008
~1040
C
~1050
D
~1060
C ⊕ D
REFERENCE
1012
1014
~1070

FIGURE 10

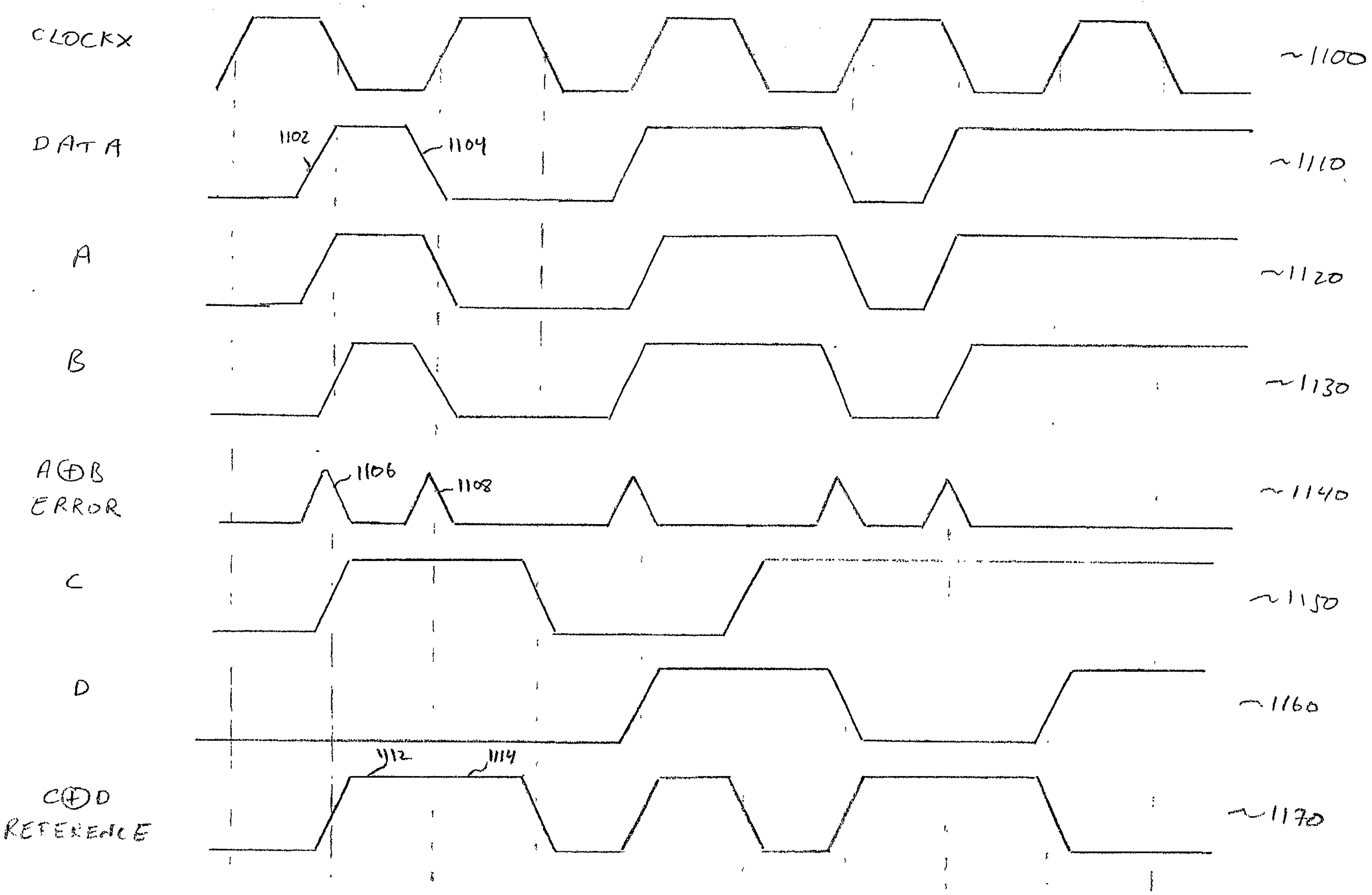
CLOCKX
~1100
DATA
1102
1104
~1110
A
~1120
B
~1130
A⊕B ERROR
1106
1108
~1140
C
~1150
D
~1160
C⊕D REFERENCE
1112
1114
~1170

Figure 11

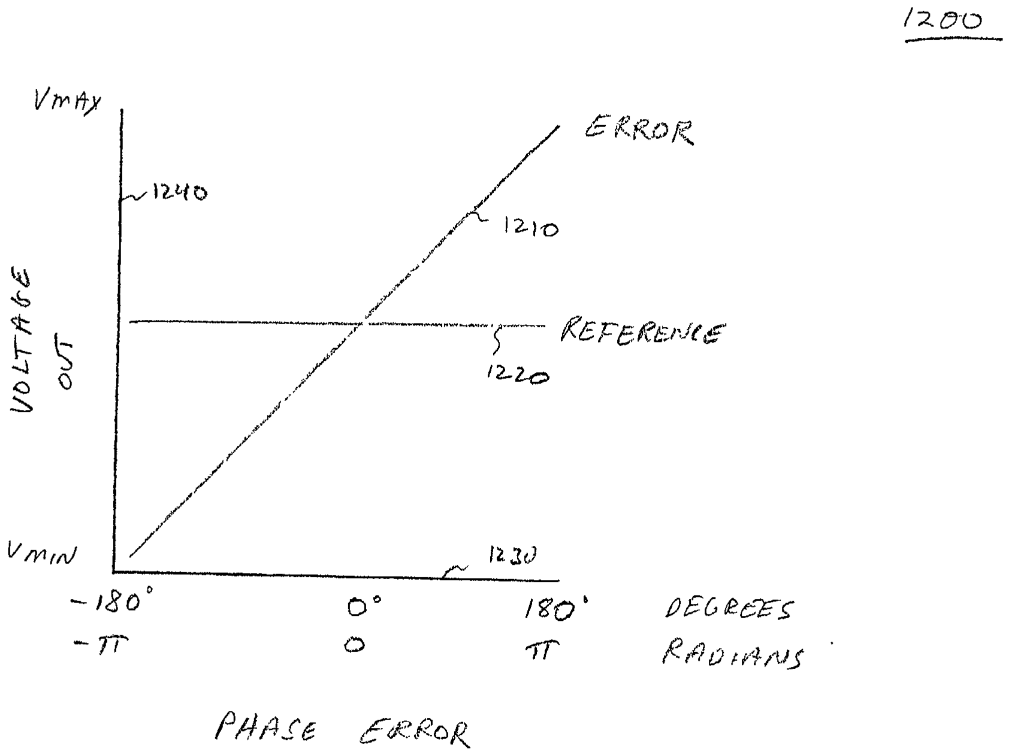
1200
VMAX
VMIN
VOLTAGE OUT
1240
1210
ERROR
REFERENCE
1220
1230
-180°
0°
180°
DEGREES
-π
0
π
RADIANS
PHASE ERROR

FIGURE 12

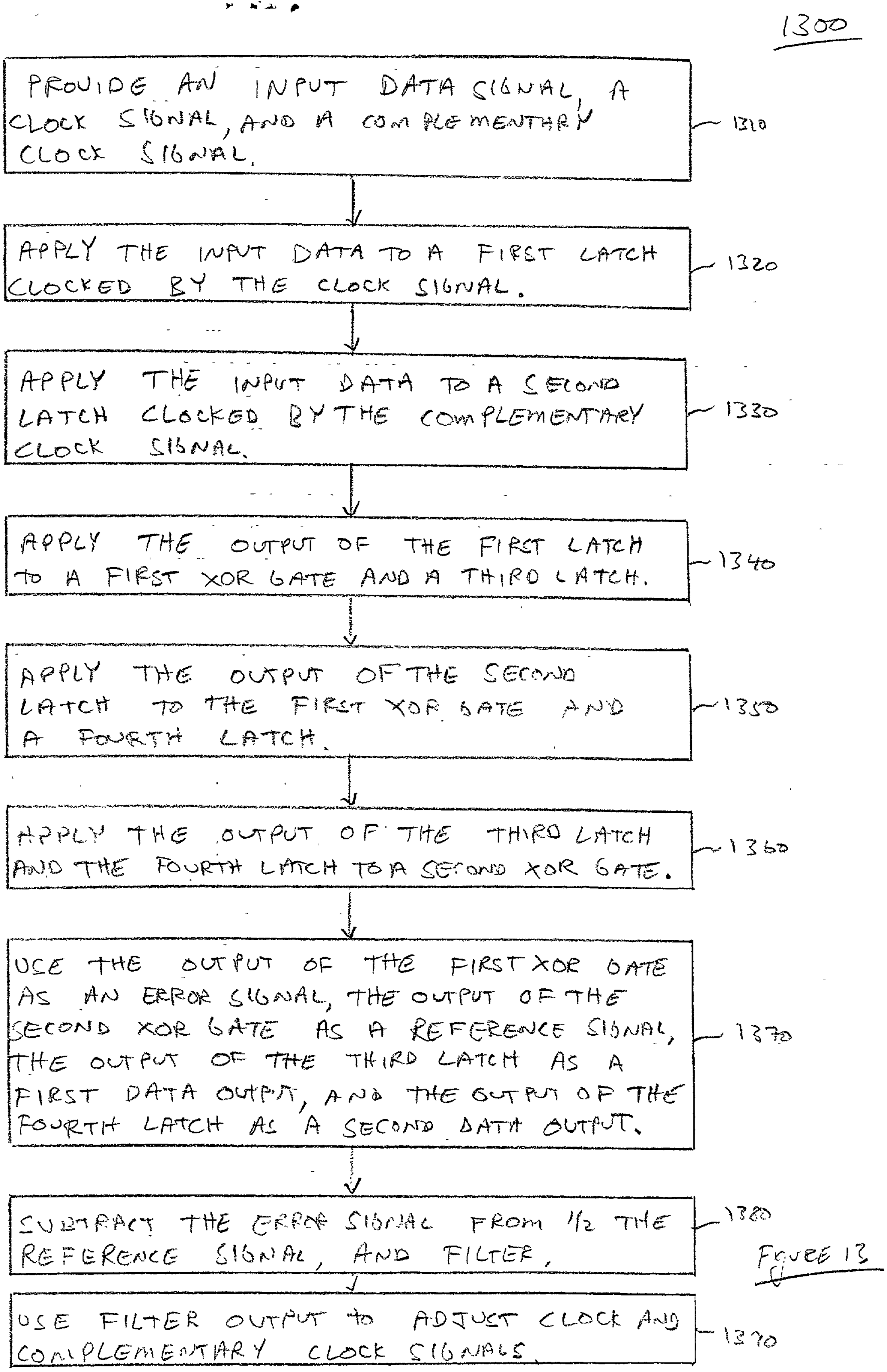
1300
PROVIDE AN INPUT DATA SIGNAL, A CLOCK SIGNAL, AND A COMPLEMENTARY CLOCK SIGNAL.
1310
APPLY THE INPUT DATA TO A FIRST LATCH CLOCKED BY THE CLOCK SIGNAL.
1320
APPLY THE INPUT DATA TO A SECOND LATCH CLOCKED BY THE COMPLEMENTARY CLOCK SIGNAL.
1330
APPLY THE OUTPUT OF THE FIRST LATCH TO A FIRST XOR GATE AND A THIRD LATCH.
1340
APPLY THE OUTPUT OF THE SECOND LATCH TO THE FIRST XOR GATE AND A FOURTH LATCH.
1350
APPLY THE OUTPUT OF THE THIRD LATCH AND THE FOURTH LATCH TO A SECOND XOR GATE.
1360
USE THE OUTPUT OF THE FIRST XOR GATE AS AN ERROR SIGNAL, THE OUTPUT OF THE SECOND XOR GATE AS A REFERENCE SIGNAL, THE OUTPUT OF THE THIRD LATCH AS A FIRST DATA OUTPUT, AND THE OUTPUT OF THE FOURTH LATCH AS A SECOND DATA OUTPUT.
1370
SUBTRACT THE ERROR SIGNAL FROM 1/2 THE REFERENCE SIGNAL, AND FILTER.
1380
USE FILTER OUTPUT TO ADJUST CLOCK AND COMPLEMENTARY CLOCK SIGNALS.
1390

FIGURE 13